A New Single-Phase to Three-Phase Adjustable Speed Drive Based on Z-Source Inverter

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Abstract:

Three-phase to three-phase Adjustable Speed Drive (ASD) was widely studied for motor drives. This paper proposed a new single-phase to three-phase ASD system based on Z-source inverter. The Z-source inverter system has a unique X-shape of two LC network between in the frontend of the diode rectifier and the AC side. By controlling the shoot-through duty cycle, the Z-source can produce any desired output AC voltage. The overall system model and control is illustrated two control strategies are designed and investigated. As results the new proposed Z-source system provides ride-through capability during voltage sags, reduces source harmonics, reduces input voltage ripple, reduces hardware complexity, and extends output voltage range. Analysis and simulation results will be presented to demonstrate these features.

Keywords: Z-source inverter, shoot-through, ride-through, PID controller, voltage mode control.

1. Introduction:

The conventional adjustable speed motor drive generally uses voltage source inverter VSI which consist of a fronted Diode Bridge Rectifier, DC-link, LC filter and inverter Bridge. The maximum output voltage can be obtained from this drive depends on the value of the DC-link, for example; if the input line-to-line voltage of the drive is 380V. The average value of the DC-link is 537V DC, which is roughly 1.41 times the line-to-line input voltage under light load condition, under which the inverter can only produce a maximum output line-to-line voltage about 305V AC. Therefore the VSI is a step-dawn converter.

When a single phase input source is used for AC drive the value of the DC link falls dawn to the average value: $2V_m/\pi = 200$V DC, under which the inverter can only produce a maximum output line-to-line voltage about 118V AC. Moreover, the voltage sags can interrupt an ASD system and shutdown critical loads and processes. The DC capacitor in an ASD is a relatively small energy storage element, which cannot hold DC voltage above the operable level under such voltage sags [1, 2]. Lack of ride-through capacity is a serious problem for sensitive loads driven by ASDs. Usually an additional boost converter is added to energies the DC link to the desired level and to achieve ride-through [3], as shown in figure (1). This solution tends to increase system cost, size and complexity. Moreover this boost converter has highly unstable performance under load variation.

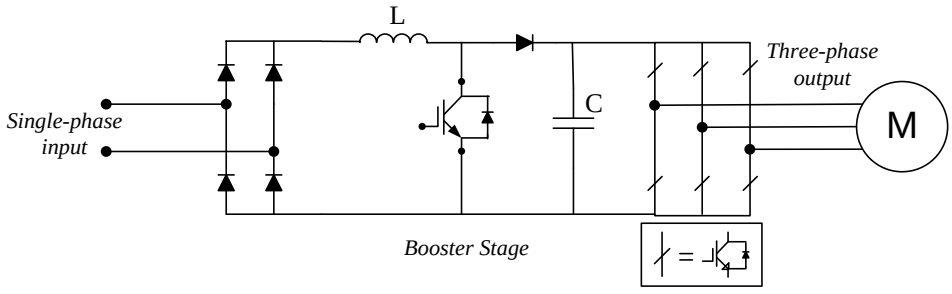


Figure (1) Booster Stage plus VSI

Nowadays Z-Source Inverter or (Impedance source), which firstly presented by Fang Zheng Peng 2003 [4], gives good solutions for many problems that VSI is suffered from. A Z-source ASD can: [5]

i- Provide ride-through driving voltage sags without any additional circuit.
ii- Produce any desired output ac voltage even greater than the input line voltage.
iii- Improve power factor and thermal current and common mode voltage.

This paper proposes the Z-source inverter as a single stage booster-inverter for single-phase to three-phase ASD. Simulation and results and included to prove the concept and feature of the new ASD system.

2. Z-Source Inverter Operating Principles:

The general Z-source inverter structure is a two part network that consist of a split of inductor L1 and L2 and capacitors C_1 and C_2 connected in X-shape is employed to provide an impedance source (Z-source) coupling the inverter side to the input power source. The basic operating principle and control of the Z-source inverter fed by a DC source as fuel cell stack have been detailed in [4]. In the proposed ASD system a diode rectifier bridge provided with input capacitor (C_s) serves as a DC source feeding the Z-source network as shown in figure (2).

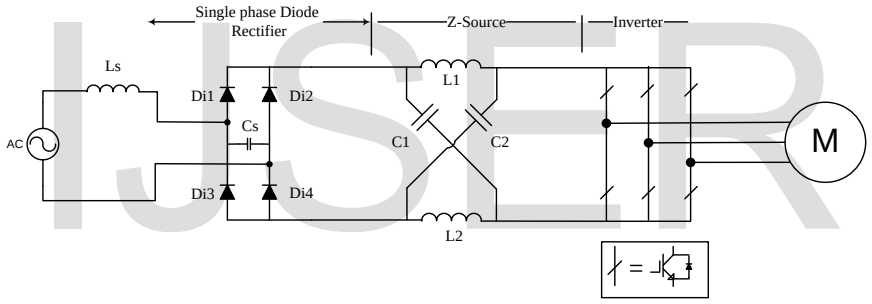


Figure (2) Single-Phase to Three-Phase Z-Source Inverter

This Z-source coupling provides unique features that cannot be achieved from traditional VSI and overcome many limitations [6]. Traditional VSI has eight switching states (vectors), six active vectors when the DC voltage is impressed across the load and two zero vectors when the load terminals are shorted through eight the lower or upper three devices, respectively. The most important condition that is the lower device should be inverted of the upper device state. The dead time to block the upper and lower devices of the same phase leg has to be provided to prevent a short circuit. Unlike traditional VSI, the three phase Z-source inverter has nine permissible switching vectors; the previous eight states and one extra zero vector when the load terminals are shorted through both the upper and lower devices of any one phase leg (i.e. both devices are gating on), any two phase legs, or all three phase legs. This ninth vector called shoot-through zero state, which can be generated by seven different ways: shoot-through via any one phase leg, combinations of any two phase legs, and all three phase legs. This shoot-through zero state provides the unique buck-boost feature to the inverter [4]. The input capacitors are used to suppress voltage surge that may occur due to the line inductance during diode commutation and shoot-through mode of the inverter, thus requiring a small value of a capacitance. At the first half cycle the two diodes Di_1 and Di_4 are conduct with the capacitor C_s. Therefore as viewed from the

Z-source network, the capacitor C_s and the diode bridge can be modeled a DC-source in series with two diodes.

Furthermore, the two diodes conduct in series acting like one when viewed from the Z-source network. As a result, the proposed Z-source ASD system is reduced to the basic Z-source inverter has been presented in [4] which have three operating modes depending on the inverter bridge′s switching state: (assume that the input source is in the first half cycle)

i. Mode-1 (*or active mode*):

This mode occurs when the inverter bridge is operating in one of the six traditional active vectors, thus it acting as current source (i_s) viewed from the Z-source circuit. Figure (3) shows the circuit of this mode. Z-source circuit always forces (Di_1 and Di_4) to conduct and carry the current difference between the inductor current (I_L) and inverter DC current (i_s); ($2I_L$-i_s). Both inductors have an identical current value because of the circuit symmetry. This unique feature wide the line current conducting intervals, thus reduce harmonic current [5].

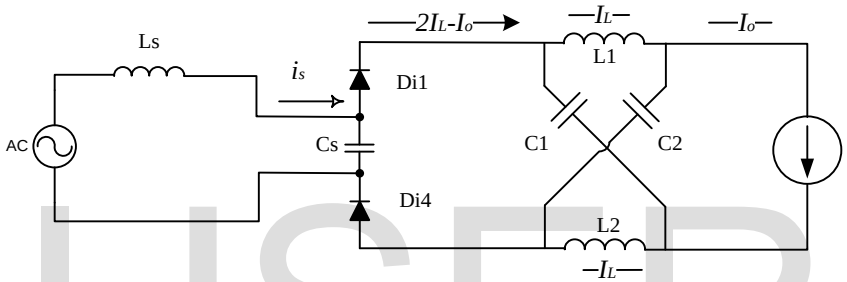


Figure (3) Mode-1

ii. Mode-2 (*or shoot-through mode*):

This mode occurs when the inverter bridge is operating in one of the seven shoot-through state. During this mode, both diodes are off separating the DC link from the ac line. The line current flows to the capacitor C_s [5], as shown in figure (4). Depending on how much a voltage boost is needed, the shoot-through interval (T_{sh}) or its duty cycle (T_{sh}/T) is determined [4].

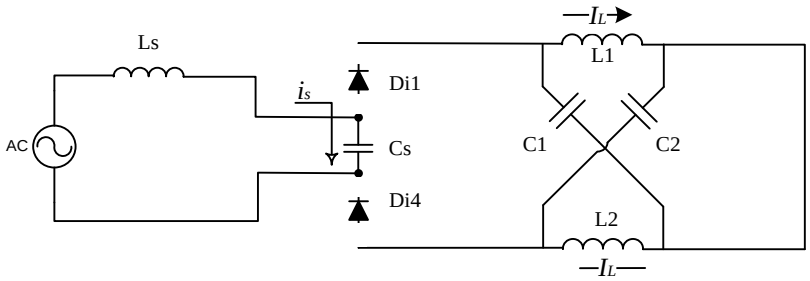


Figure (4) Mode-3

All relationships described in detail [4] about the DC capacitor voltage, shoot-through time interval (or duty cycle), and output voltage held true for the proposed ASD system except the value of (V_{in})

$$V_{c1}=V_{c2}=V_c=\frac{1-\frac{T_{sh}}{T}}{1-2\frac{T_{sh}}{T}}=\frac{B+1}{2}V_{in} \quad (1)$$

$$\tilde{V}_{ac}=MB\frac{V_{in}}{2} \quad (2)$$

$$B=\frac{1}{1-2\frac{T_{sh}}{T}} \quad (3)$$

$$V_{in}=\frac{2}{\pi}\sqrt{2}\,V_{rms} \quad (4)$$

$$V_{out}=B\,V_{in}=\frac{2B}{B+1}V_c \quad (5)$$

Where V_{C1} and V_{C2} are voltages across the DC capacitors C_1 and C_2 and have and an equal values because of the symmetry of the circuit. T_{sh} is the shoot-through interval over one switching cycle T. $\tilde{V}_{ac}$ is the peak voltage produced by the inverter, B is the boosting factor and M is the modulation index of the inverter, V_{in} is the inherent DC voltage of the rectifier fed from the single phase line voltage V_{rms}, V_{out} is the equivalent DC-link voltage across the inverter bridge.

4. Mathematical modeling of Z-source Inverter:

4.1. Equivalent Switching Circuit of ZSI:

The two non-zero operation modes of the ZSI network involving two different circuit topologies, these two circuits can be summarized in one equivalent circuit which can represents the ZSI operation modes as shown in figure (5).

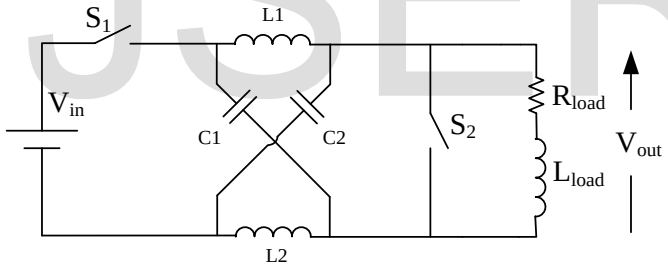


Figure (5) Equivalent Switching Circuit of ZSI Network

In mode-1; S_1-off and S_2-on, there is no energy transferred from the source to the load, because the load side and source side are essentially decoupled by the shoot-through state and the open states of S_1.

In mode-2; S_1-on and S_2-off, the real energy will be transferred from the source to the load due to the conduct of S_1 and absence of shoot-through state.

Both of control-to-output and disturbance-to-output voltage transfer functions can be obtained by using small signal modeling based on the following assumptions: the ZSI is operating in continuous condition mod, the passive components in the Z-network are lossless and the load current is continuous because of an inductive load. The AC side circuit can be simplified to an equivalent DC load $Z_{load} = R_{load} + j\omega L_{load}$; where R_{load} is calculated by power balance as $R_{load} = 8|Z_{load}|/3\cos\varphi$ and L_{load} is determined so that the time constant of the DC load is the same as the AC load [11].

The state variables of the system can be defined as: $i_{L1}(t)$, $i_{L2}(t)$, $v_{C1}(t)$, $v_{C2}(t)$. The input voltage $V_{in}(t)$ is independent voltage source. The state space equations of mode-1 can be written as:[12]

$$\begin{bmatrix} L_1 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 \\ 0 & 0 & C_1 & 0 \\ 0 & 0 & 0 & C_2 \end{bmatrix} \begin{bmatrix} \nabla i_{L1}(t) \\ \nabla i_{L2}(t) \\ \nabla v_{c1}(t) \\ \nabla v_{c2}(t) \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ -1 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{l2}(t) \\ v_{c1}(t) \\ v_{c2}(t) \end{bmatrix} \quad (6)$$

Where: ∇ represents d/dt

The state space equations of mode-2 are:

$$\begin{bmatrix} L_1 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 \\ 0 & 0 & C_1 & 0 \\ 0 & 0 & 0 & C_2 \end{bmatrix} \begin{bmatrix} \nabla i_{L1}(t) \\ \nabla i_{L2}(t) \\ \nabla v_{c1}(t) \\ \nabla v_{c2}(t) \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & -1 \\ 0 & 0 & -1 & 0 \\ 0 & 1 & \frac{-1}{Z_{load}} & \frac{-1}{Z_{load}} \\ 0 & -1 & \frac{-1}{Z_{load}} & \frac{-1}{Z_{load}} \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{l2}(t) \\ v_{c1}(t) \\ v_{c2}(t) \end{bmatrix} + \begin{bmatrix} 1 \\ 1 \\ \frac{-1}{Z_{load}} \\ \frac{-1}{Z_{load}} \end{bmatrix} V_{in}(t) \quad (7)$$

4.2. AC Small Signal Modeling of ZSI Based on State Space Averaging:

The small signal relationship among the state variables is derived by applying small signal perturbations $\tilde{v}_{in}(t)$ to the input voltage, and $\tilde{d}(t)$ to the shoot-through duty ratio (D_1) shown by $v_{in}(t) = V_{in} + \tilde{v}_{in}(t)$ and $d(t) = D_1 + \tilde{d}(t)$ [13]. The perturbations result in small signal variations in the state variables $x = X + \tilde{x}$. Combing mode-1 and mode-2 equations and by using state space averaging method, the averaged matrix is [14]:

$$\begin{bmatrix} L_1 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 \\ 0 & 0 & C_1 & 0 \\ 0 & 0 & 0 & C_2 \end{bmatrix} \begin{bmatrix} \nabla \tilde{i}_{L1}(t) \\ \nabla \tilde{i}_{L2}(t) \\ \nabla \tilde{v}_{c1}(t) \\ \nabla \tilde{v}_{c2}(t) \end{bmatrix} = \begin{bmatrix} 0 & 0 & D_1 & -D_2 \\ 0 & 0 & -D_2 & D_1 \\ -D_1 & D_2 & \frac{-D_2}{Z_{load}} & \frac{-D_2}{Z_{load}} \\ D_2 & -1 & \frac{-D_2}{Z_{load}} & \frac{-D_2}{Z_{load}} \end{bmatrix} \begin{bmatrix} \tilde{i}_{L1}(t) \\ \tilde{i}_{l2}(t) \\ \tilde{v}_{c1}(t) \\ \tilde{v}_{c2}(t) \end{bmatrix} + \begin{bmatrix} D_2 \\ D_2 \\ \frac{D_2}{Z_{load}} \\ \frac{D_2}{Z_{load}} \end{bmatrix} V_{in}(t) +$$

$$\begin{bmatrix} V_{c1} + V_{c2} - V_{in} \\ V_{c1} + V_{c2} - V_{in} \\ -I_{L1} - I_{L2} + \frac{V_{c1}}{Z_{load}} + \frac{V_{c2}}{Z_{load}} + \frac{V_{in}}{Z_{load}} \\ -I_{L1} - I_{L2} + \frac{V_{c1}}{Z_{load}} + \frac{V_{c2}}{Z_{load}} + \frac{V_{in}}{Z_{load}} \end{bmatrix} \tilde{d}(t) \quad (8)$$

Where: D_1 is mode-1 duty cycle duty cycle, D_2 mode-2 duty cycle, I_{L1}, I_{L2}, V_{C1}, V_{C2} and V_{in} are DC steady state values.

Taking Laplace transformation and solving of the above equations, the capacitor output voltage can be derived [14]:

$$\tilde{v}_c(s) = G_{V_{c/d}}(s).\tilde{d}_1(s) + G_{V_{c/in}}(s).\tilde{v}_{in}(s) \quad (9)$$

Where:

$$G_{V_{c/d}}(s) = \frac{\tilde{v}_c(s)}{\tilde{d}(s)} \Big|_{\tilde{v}_{in}=0} = \frac{\left(-2\, I_L + \frac{2V_C - V_{in}}{R_{load}}\right).LS + (D_2 - D_1).(2V_C - V_{in})}{LCS^2 + \frac{2D_2 L}{Zload} S + (D_1 - D_2)^2} \quad (10)$$

And

$$G_{V_{c/in}}(s) = \frac{\tilde{v}_c(s)}{\tilde{v}_{in}(s)} \Big|_{\tilde{d}(s)=0} = \frac{\frac{D_2 L}{Z_{load}} S + D_2(D_2 - D_1)}{LCS^2 + \frac{2 D_2 L}{Zload} S + (D_1 - D_2)^2} \quad (11)$$

Substituting $Z_{load}(s) = R_{load} + S L_{load}$ gives:

$$G_{V_{c/d}}(s) = \frac{b_0 S^2 + b_1 S + b_2}{a_0 S^3 + a_1 S^2 + a_2 S + a_3} \quad (12)$$

$$G_{V_{c/in}}(s) = \frac{h_0 S + h_1}{a_0 S^3 + a_1 S^2 + a_2 S + a_3} \quad (13)$$

Where:

$a_o = L\ L_{load}\ C$

$a_1 = R_{load}\ L\ C$

$a_2 = 2\ D_2\ L + L_{load}\ (D_1 - D_2)^2$

$a_3 = R_{load}\ (D_1 - D_2)^2$

$b_o = (-2\ L_{load} + \frac{2 V_c - V_{in}}{R_{load}})\ .\ L\ .\ i_L$

$b_1 = -2\ R_{load}\ L\ I_{load} + (2 V_c - V_{in}).L + (2 V_c - V_{in})\ (D_2 - D_1)\ i_{load}$

$b_2 = (D_2 - D_1).\ (2 V_c - V_{in}).\ R_{load}$

$h_0 = D_2\ (D_2 - D_1)\ L_{load} + D_2\ L$

$h_1 = D_2\ (D_2 - D_1)\ R_{load}$

5. Selection of L & C:

Obviously, from equations (12) and (13) that the RHP zero and pole locations in the s-domain depend on Z-network parameter (L and C) and the control input D_1 variation causing movement of the poles and zeros. These movements would result in unsatisfactorily oscillatory and non-minimum-phase responses especially for sources with wide operating ranges. Therefore selecting of Z-network parameters is very important to obtain stable response and reduces oscillation. To investigate the level of pole-zero sensitivity parameters sweep is used by changing a particular parameter with the others kept constant at the nominal values: V_{in}=198V, L=500µH, C=500µF, D_1=0.3. The pole-zero trajectories in the S-domain are plotted for each variation steps.

By increasing Z-network capacitor C from 100µF to 200µF, the poles are shifted vertically towards the real axis, while the RHP zero stays relatively unchanged as shown in figure (6). Since the effect of changing C shifting the poles only then it considered to increase the system damping and reduce over-shoot but an increased rise-time.

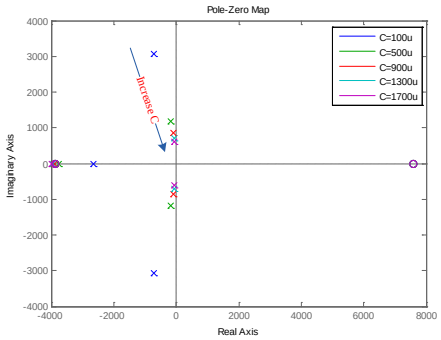


Figure (6) Pole-Zero Map of the ZSI (Sweeping Capacitance)

By the same way sweeping Z-source inductor L from 50μH to 500μH leads to shifting the poles and RHP zero towards the imaginary axis. The shifting of zero increases the non-minimum-phase response, while the shifting of poles increases the system setting time and oscillatory response.

This analysis show that although large values of L and C give rise to low steady state voltage and current ripples, and generally give rise to inferior transient response. Thus, a compromising approach must be taken depending and the particular applications.

Now eventually the choice of L and C can be made from a series of tradeoffs among the following considerations:

- Proper quality factor and damping factors.
- Smaller passive components (lower costs and sizes).
- Sufficient phase margins for closed loop control.
- Satisfactory ripple performance.
- Resonant frequency for away from the z-network switching frequency for stability.

According to the above analysis it is suggested that L be a value of 250μH and C 470μF. Using this parameters further investigation of L and C in the Z network can be done by using computer simulation. Figure (7) shows the simulated capacitor voltage of ZSI when subjected to 10% step change in the shoot-through duty ratio from 0.3 to 0.33 at t=0.2 second. The varies combinations of L and C are: (a) L=150μH, C=470 μF. (b) L=250 μH, C=470 μF. (c) L=250 μH, C=1000 μF. The results confirm that the choice of L and C is suitable.

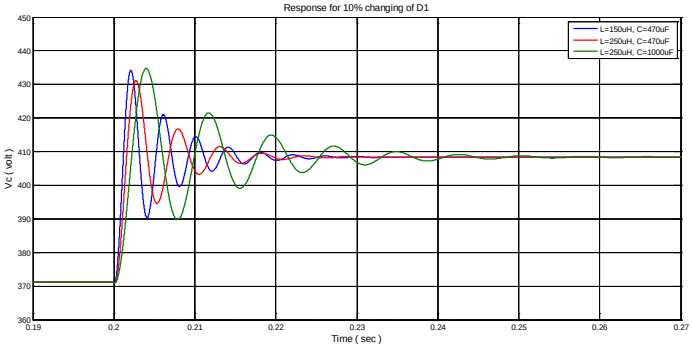


Figure (7) Capacitor Voltage Response of ZSC When Subjected To 10% Step Change in Duty Ratio for Various Combinations of L&C

6. Control Strategies:

Voltage mode closed loop control is used to control the output voltage of the ZSI to the desired value. Generally there are two main control strategies; direct and indirect control.

6.1. Indirect control of ZSI:

The DC-link voltage v_{out} is the square waveform due to the operating modes. This has zero value during the shoot-through state and it has peak value v_{out} during non-shoot-through state. Therefore, the peak DC-link voltage is not suitable for used as a feedback signal [15]. Most papers used the Z-source capacitor voltage as a feedback, because of its continuity, to estimate the error signal between the capacitor voltage and reference value, and then control the duty ratio d1 through PID controller to obtain constant capacitor voltage as shown in figure (8). It is obvious that by controlling only the capacitor voltage, the DC-link voltage is open to disturbances coming from the input voltage. This effect could be transferred to the output side, which distorts the output voltage and increase the output voltage stress across the switches.

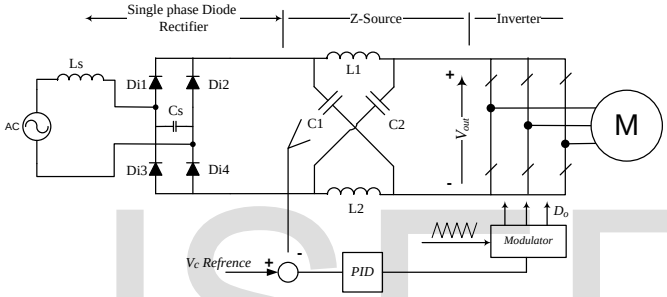


Figure (8) Indirect Control of ZSI

6.2. Direct Control of ZSI:

The peak DC-link voltage which has a square waveform can be measured (or detect) by using a peak detection circuit. The measurement signal, which is no more pulsating, can be used as a feedback signal as shown in figure (9). The non-zero value of the dc-link voltage $v_{dc\text{-}peak}$ (peak dc-link voltage) is a linear combination of the capacitor voltage which is state variable and the input voltage ($v_{dc\text{-}peak} = 2v_c\text{-}v_{in}$) [16]. In steady state operation the capacitor voltage and the input voltage are continuous signals. Although the DC-link voltage v_{out} itself is a pulsating waveform, the peak value of the DC-link voltage $v_{dc\text{-}peak}$ can be obtained as a continuous signal.

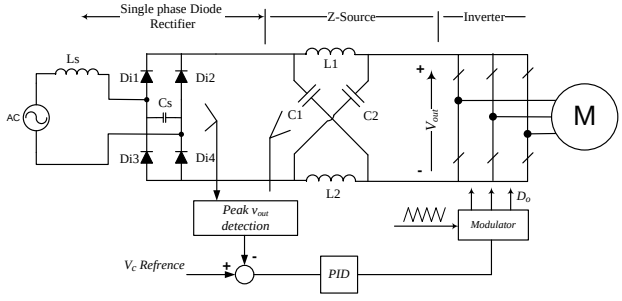


Figure (9) Direct Control of ZSI

7. Design of PID Controller:

The transfer function of the control-to-output shows that DC side of Z-source inverter has non-minimum phase characteristics. In order to compensate the low-frequency loop gain and improving phase margin, a PID compensator has been used to compensate the control-to-output transfer function and control the capacitor voltage. The Bode plot of the uncompensated loop gain is sketched in figure (10).

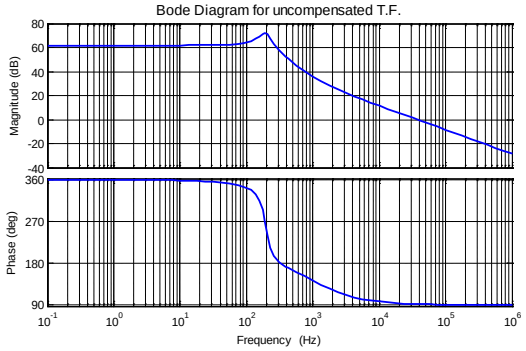


Figure (10) Bode Plot of the Uncompensated System

Obviously, the uncompensated loop gain has crossover frequency f_c=40KHz with negative phase margin φ_m = -85°.The used component parameters of the system for controller design are: V_{in}=198, C=470μF, L=250μH, D=0.3, f=10 KHz. The transfer function of the designed PID controller $G_c(s)$ is:

$$G_c(s) = K_c \frac{(1+\frac{S}{w_z})(1+\frac{w_L}{S})}{(1+\frac{S}{w_p})} \quad (14)$$

A new crossover frequency (f_c) has been chosen to be one tenth of switching frequency in order to avoid oscillation f_c=1 KHz. The orbitary value of the phase margin has been chosen about φ_m=60°, then pole and zero frequencies of the PD part of the compensator $G_c(s)$ are:

$$w_z = w_c \sqrt{\frac{1-\sin(\theta_m)}{1+\sin(\theta_m)}} \quad (15)$$

$$w_p = w_c \sqrt{\frac{1+\sin(\theta_m)}{1-\sin(\theta_m)}} \quad (16)$$

Consequently, the invented zero of the PI part of the compensator $G_c(s)$ has been chosen to be one tenth of the crossover frequency f_L=100Hz, finally the PID controller gain K_c can be determined as:

$$K_c = \left| \frac{1}{G_{V_{c/d}}(s)\ Gc(s)} \right|_{w=w_c} \quad (17)$$

Figure (11) shows the bode plot of the compensator ZSI the system has a phase margin about (55°) and gain margin of (18dB) and crossover frequency (1KHz).

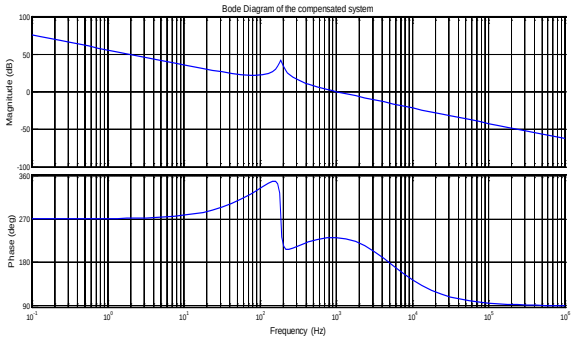
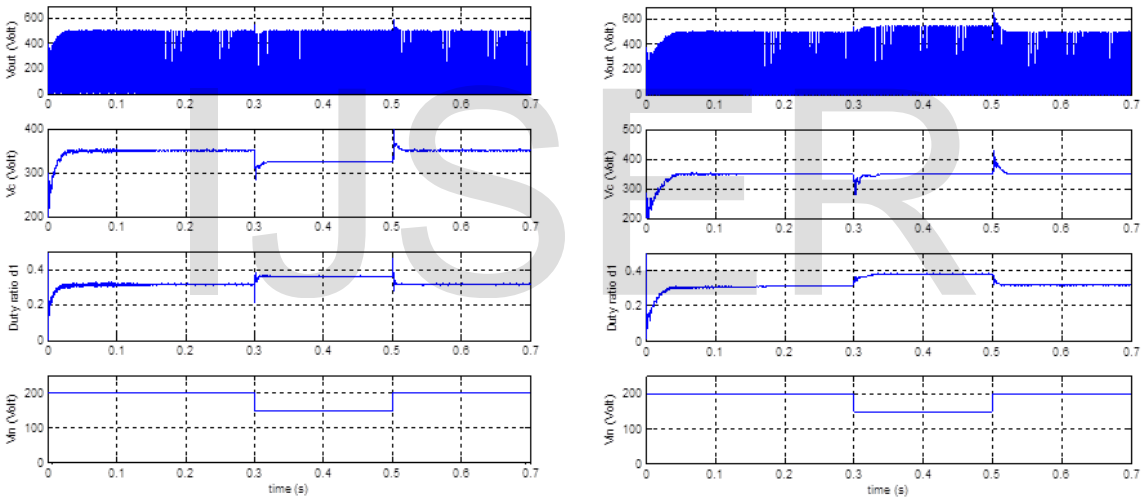


Figure (11) Bode Plot of the Compensated System

To examine the effectiveness of the designed PID controller for both direct and indirect strategies, an external pure DC source is used to reduce the effect of input voltage ripple. The simulation results give good dynamic performance under 25% changes in the input voltage for both direct and indirect controllers as shown in figure (12).



(a) (b)

Figure (12) System Performance Under 25% Change of Input Voltage.
(a) Direct Control, (b) Indirect Control

8. Simulation Results:

Simulation results have been carried out to improve the concept and verify the features of the proposed single-phase to three-phase ASD system for both direct and indirect DC-link PID controller. System parameters used in the simulation are: V_{in}=220rms, C=470μF, L=250μH, D=0.3, 3-φ 7hp 400V 50Hz 4-pole induction motor.

Figure (13) shows the simulated v_{out} , v_c , d1 and v_{in} waveform in the case of input voltage sag of 20% when indirect control is used. It can be seen that the input disturbance effects the DC-link voltage and increase the peak value of it, which may increase the voltage stress of the switching

devise, while the capacitor voltage remain constant at the desired value due to controlling the shoot-through duty cycle d_1. Figure (14) shows the AC side performance: voltage, motor current and motor speed. It can be seen that the input voltage ripple is partly illuminated in the DC-link by the control loop but the peak output voltage is increase during the voltage sag period, which many causes saturation due to current increasing.

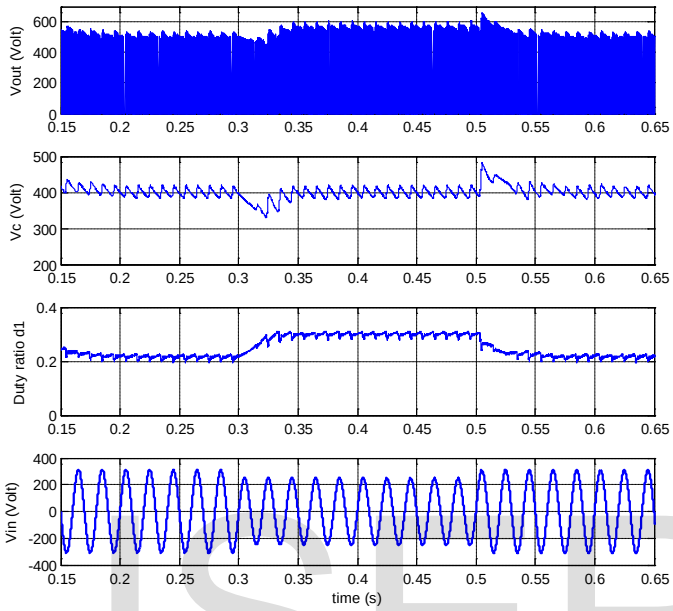


Figure (13) DC Side of the ZSI Indirect Control

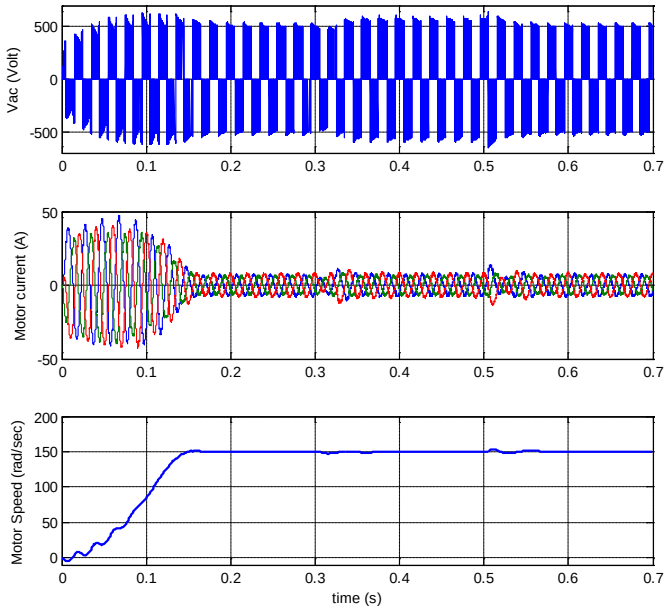


Figure (14) AC Side and Motor Performance under Indirect Control

Figures (15) and (16) show the DC and AC side performances of the Z-source inverter and the induction motor under direct control strategy. It obviously that the DC-link voltage is remain constant during 20% input voltage sag duration, while the capacitor voltage is free to disturbance. Direct control gives constant output AC voltage and stable operation behavior of the induction motor during input voltage sag.

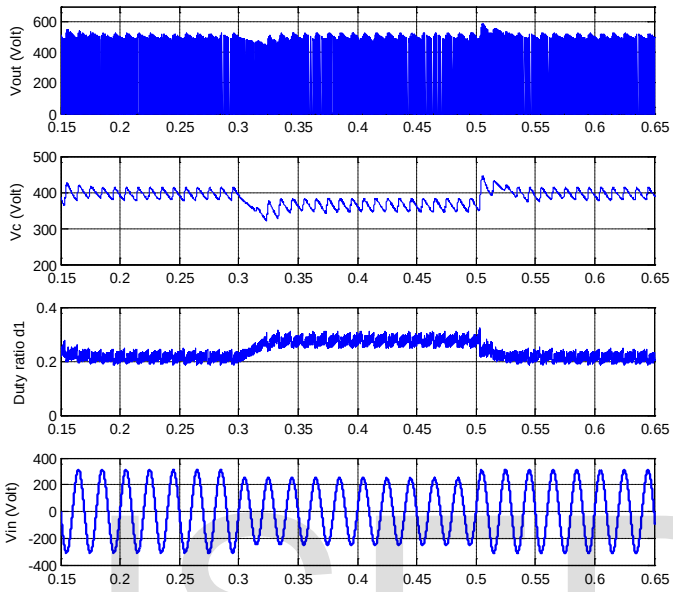


Figure (15) Direct Control of the ZSI

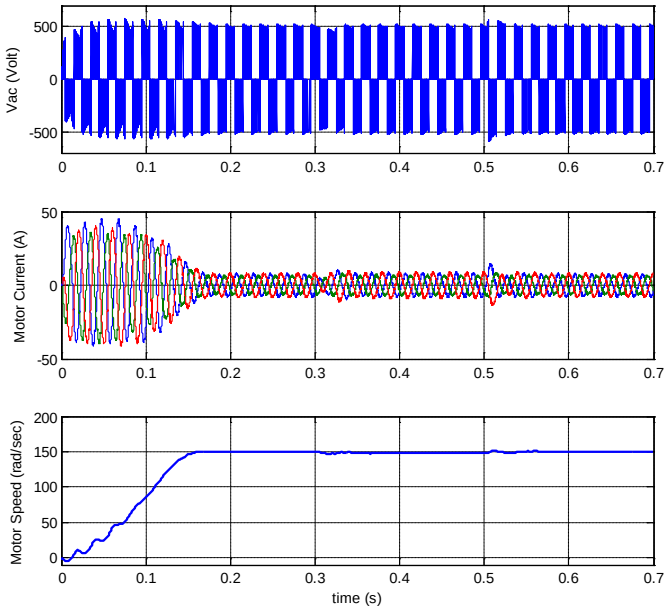


Figure (16) Induction Motor Performance under Direct Control

9. Conclusion:

This paper presents a new single-phase to three-phase adjustable speed drive system based on the Z-source inverter. The operating principle and analysis have been given. Simulation results verified the features of the proposed ASD system which can be summarized as follows:

1- The peak input voltage is boosted to the desired dc-link within the Z-source inverter.
2- Overcome the effect of voltage sags without using additional booster circuit.
3- Source current harmonics are reduced by the Z-network inductance.
4- Reduce input DC voltage ripple within the Z-network.
5- The indirect control is a simple controlling method, but it cannot control the DC-link voltage which may cause undesired system operation by further increasing of the motor voltage and current.
6- The direct control can controls the DC-link voltage by additional peak detection circuit which gives good operation performance.

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